AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Original) A temperature and process independent analog integrated circuit comprising:

an analog function core responsive to a first differential input signal and a second differential input signal, and having first and second output terminals;

a first loading device having a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal;

a second loading device having a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal; and

a compensation circuit in communication with said first and second control terminals,

wherein said compensation circuit comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals; and

a first differential amplifier having a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

2. (Previously Presented) The temperature and process independent analog integrated circuit of claim 1 wherein said analog function core is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

3. (Previously Presented) The temperature and process independent analog integrated circuit of claim 1 wherein the analog function core is a multiplier circuit comprising:

a first current source;

a second current source;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains in communication with the first current source, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains in communication with the second current source, and commonly connected second sources;

a third current source in communication with the commonly connected first sources to form the first output terminal; and

a fourth current source in communication with the commonly connected second sources to form the second output terminal.

4. (Previously Presented) The temperature and process independent analog integrated circuit of claim 1 wherein the first and second loading devices comprise MOS transistors.

5. (Previously Presented) The temperature and process independent analog integrated circuit of claim 1 wherein said compensation circuit further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage source, and an output in communication with the second gate.

6. (Previously Presented) The temperature and process independent analog integrated circuit of claim 5 wherein the first MOS transistor and the first and second loading devices are of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

7. (Previously Presented) The temperature and process independent analog integrated circuit of claim 1 further comprising a biasing circuit to provide the common mode voltage to the first and second loading devices.

8. (Previously Presented) The temperature and process independent analog integrated circuit of claim 5 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide the second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide the third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

9. (Previously Presented) The temperature and process independent analog integrated circuit of claim 7 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

10. (Original) A temperature and process independent analog multiplier circuit comprising:

a multiplier core responsive to a first differential input signal and a second differential input signal, and having first and second output terminals;

a first loading device having a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal;

a second loading device having a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal; and

a compensation circuit in communication with said first and second control terminals,

wherein said compensation circuit comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals; and

a first differential amplifier having a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

11. (Original) The temperature and process independent analog multiplier circuit of claim 10 wherein the multiplier core comprises:

a first current source;

a second current source;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second

terminal of the first differential input signal, commonly connected first drains in communication with the first current source, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains in communication with the second current source, and commonly connected second sources;

a third current source in communication with the commonly connected first sources to form the first output terminal; and

a fourth current source in communication with the commonly connected second sources to form the second output terminal.

12. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 10 wherein the first and second loading devices comprises MOS transistors.

13. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 10 wherein said compensation circuit further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage source, and an output in communication with the second gate.

14. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 13 wherein the first MOS transistor and the first and second loading devices are of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

15. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 11 further comprising a biasing circuit to provide the common mode voltage to the first and second loading devices.

16. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 13 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide a second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide a third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

17. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 15 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

18. (Previously Presented) A temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process, said temperature and process compensation circuit comprising:

a first MOS transistor having a first source in communication with a common mode voltage, a first drain, and a first gate in communication with the control terminals;

a first differential amplifier having a first input in communication with a first bias voltage, a second input in communication with the first drain, and an output in communication with the control terminals;

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor having a third gate in communication with a second bias voltage, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input connected to the third drain and the second source, a third input in communication with a third bias voltage, and an output in communication with the second gate.

19. (Previously Presented) The temperature and process compensation circuit of claim 18 wherein the first MOS transistor is of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

20. (Previously Presented) The temperature and process compensation circuit of claim 18 further comprising a biasing circuit to provide the common mode voltage and to provide the first bias voltage, second bias voltage, and third bias voltage to said temperature and process compensation circuit.

21. (Previously Presented) The temperature and process compensation circuit of claim 20 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide the first bias voltage to the first differential amplifier that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide the second bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide the third bias voltage to the second differential amplifier that is referenced to a semiconductor bandgap voltage.

22. (Currently Amended) A temperature and process independent analog integrated circuit comprising:

analog integrated function means for providing first and second output signals responsive to a first differential input signal <u>pair</u> and a second differential input <u>signal pair</u>;

first loading means for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal;

second loading means for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and compensation means for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

23. (Previously Presented) The temperature and process independent analog integrated circuit of claim 22 wherein said analog integrated function means is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

24. (Currently Amended) The temperature and process independent analog integrated circuit of claim 22 wherein the analog integrated function means is a multiplier circuit comprising:

first current means for supplying a first current; second current means for supplying a second current;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal pair, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal pair, commonly connected first drains responsive to the first current, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal pair, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal pair, commonly connected second drains responsive to the second current, and commonly connected second sources;

third current means for supplying a third current and in communication with the commonly connected first sources to form the first output terminal; and

fourth current means for supplying a third current and in communication with the commonly connected second sources to form the second output terminal.

25. (Previously Presented) The temperature and process independent analog integrated circuit of claim 22 wherein the first and second loading means comprise MOS transistors.

26. (Previously Presented) The temperature and process independent analog integrated circuit of claim 22 wherein said compensation means comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, wherein an output of the first differential amplifier means and a signal from the first gate form the compensation control signal.

27. (Previously Presented) The temperature and process independent analog integrated circuit of claim 26 wherein said compensation means further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

28. (Previously Presented) The temperature and process independent analog integrated circuit of claim 27 wherein the first MOS transistor and the first and second loading devices are of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

29. (Previously Presented) The temperature and process independent analog integrated circuit of claim 22 further comprising biasing means to provide the common mode voltage to the first and second loading means.

30. (Previously Presented) The temperature and process independent analog integrated circuit of claim 27 further comprising a biasing circuit comprising:

means for generating the common mode voltage that is referenced to a semiconductor bandgap voltage;

means for providing a first bias voltage that is referenced to the semiconductor bandgap voltage;

means for providing a second bias voltage that is referenced to a semiconductor bandgap voltage; and

means for providing a third bias voltage that is referenced to a semiconductor bandgap voltage.

31. (Previously Presented) The temperature and process independent analog integrated circuit of claim 29 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

32. (Currently Amended) A temperature and process independent analog multiplier circuit comprising:

multiplier means for multiplying a first differential input signal pair and a second differential input signal pair to provide first and second output signals;

first loading means for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal;

second loading means for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and

compensation means for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

33. (Currently Amended) The temperature and process independent analog multiplier circuit of claim 32 wherein the multiplier means comprises:

first current means for supplying a first current; second current means for supplying a second current;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal pair, a gate of the second MOS transistor in communication with a second

terminal of the first differential input signal pair, commonly connected first drains responsive to the first current, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal pair, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal pair, commonly connected second drains responsive to the second current, and commonly connected second sources;

third current means for supplying a third current and in communication with the commonly connected first sources to form the first output terminal; and

fourth current means for supplying a third current and in communication with the commonly connected second sources to form the second output terminal.

34. (Original) The temperature and process independent analog multiplier circuit of claim 32 wherein the first and second loading devices comprises MOS transistors.

35. (Original) The temperature and process independent analog multiplier circuit of claim 32 wherein said compensation means comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first

differential amplifier means and a signal from the first gate form the compensation control signal.

36. (Original) The temperature and process independent analog multiplier circuit of claim 35 wherein said compensation means further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

37. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 35 wherein the first MOS transistor and the first and second loading devices are of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

38. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 35 further comprising biasing means for providing a common mode voltage to the first and second loading means.

39. (Original) The temperature and process independent analog multiplier circuit of claim 37 further comprising biasing means comprising:

means to generate the common mode voltage that is referenced to a semiconductor bandgap voltage;

means for providing a first bias voltage that is referenced to the semiconductor bandgap voltage;

means for providing a second bias voltage that is referenced to a semiconductor bandgap voltage; and

means for providing a third bias voltage that is referenced to a semiconductor bandgap voltage.

40. (Previously Presented) The temperature and process independent analog multiplier circuit of claim 38 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

41. (Previously Presented) A temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process, said temperature and process compensation circuit comprising:

a first MOS transistor having a first source in communication with a common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first differential amplifier means and a signal from the first gate form a compensation control signal;

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

42. (Previously Presented) The temperature and process compensation circuit of claim 41 wherein the first MOS transistor is of a first conductivity type and the second and third MOS transistors are of a second conductivity type.

43. (Previously Presented) The temperature and process compensation circuit of claim 41 further comprising biasing means to provide the common mode voltage and to provide the first bias voltage source, second bias voltage source, and third bias voltage source to said temperature and process compensation circuit.

44. (Previously Presented) The temperature and process compensation circuit of claim 43 wherein said biasing means comprises:

means to generate the common mode voltage that is referenced to a semiconductor bandgap voltage;

means to generate a first bias voltage that is referenced to the semiconductor bandgap voltage;

means to generate the second bias voltage circuit that is referenced to the semiconductor bandgap voltage; and

means to generate the third bias voltage that is referenced to the semiconductor bandgap voltage.

45. (Currently Amended) An integrated circuit, comprising:

an analog function circuit;

a differential loading device in communication with a differential output of the analog function circuit;

a compensation circuit in communication with the differential loading device; and

a biasing circuit in communication with a common mode node of the differential loading device and an input of the compensation circuit,

wherein the biasing circuit provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit, and

wherein the common mode voltage is independent of temperature and manufacturing process variations, and

wherein the biasing circuit provides a plurality of control bias voltage signals to the compensation circuit.

46. (Cancelled)

47. (Currently Amended) The integrated circuit of claim ~~46~~ 45, wherein the compensation circuit provides a bias voltage to the differential loading device, and wherein the bias voltage is independent of temperature and manufacturing process variations.

48. (Previously Presented) The integrated circuit of claim 47, wherein the bias voltage varies a differential loading of the differential loading device.

49. (Previously Presented) The integrated circuit of claim 47, wherein the bias voltage is comprised of at least the common mode voltage and the plurality of control bias voltage signals.

50. (Previously Presented) The integrated circuit of claim 47, wherein the bias voltage controls a loading on at least one voltage signal associated with the differential loading device.

51. (Previously Presented) The integrated circuit of claim 47, wherein the differential loading device provides the temperature and process independent output

voltage comprised of at least a differential output signal of the analog function circuit, the common mode voltage, and the bias voltage.

52. (Currently Amended) The integrated circuit of claim ~~46~~ 45, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

53. (Previously Presented) The integrated circuit of claim 45, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

54. (Previously Presented) The integrated circuit of claim 45, wherein the analog function circuit comprises a circuit selected from the group consisting of multipliers, adaptive filters, modulators and neural networks.

55. (Previously Presented) The integrated circuit of claim 45, wherein the differential loading device comprises first and second transistors,

wherein the first transistor comprises a first terminal responsive to a first output terminal of the analog function circuit, a second terminal in communication with the common mode node, and a first control terminal,

wherein the second transistor comprises a third terminal responsive to a second output terminal of the analog function circuit, a fourth terminal in communication with the common mode node, and a second control terminal, and

wherein the biasing circuit is in communication with the first and second control terminals.

56. (Currently Amended) An integrated circuit, comprising:

an analog function means for performing an analog function;

a differential loading means for providing a differential load,

wherein the differential loading means is in communication with a differential output of the analog function means;

a compensation means for providing a compensation signal,

wherein the compensation means is in communication with the differential loading means; and

a biasing means for providing a bias signal,

wherein the biasing means is in communication with a common mode node of the differential loading means and an input of the compensation means,

wherein the biasing means provides a common mode voltage to the common mode node of the differential loading means and the compensation means, and

wherein the common mode voltage is independent of temperature and manufacturing process variations, and

wherein the biasing means comprises means for generating a plurality of control bias voltage signals for the compensation means.

57. (Cancelled)

58. (Previously Presented) The integrated circuit of claim 56, wherein the compensation means comprises means for generating a bias voltage for the differential loading means, and

wherein the bias voltage is independent of temperature and manufacturing process variations.

59. (Previously Presented) The integrated circuit of claim 58, wherein the bias voltage varies a differential loading of the differential loading means.

60. (Previously Presented) The integrated circuit of claim 58, wherein the bias voltage is comprised of at least the common mode voltage and the plurality of control bias voltage signals.

61. (Previously Presented) The integrated circuit of claim 58, wherein the bias voltage controls a loading on at least one voltage signal associated with the differential loading means.

62. (Previously Presented) The integrated circuit of claim 58, wherein the differential loading means provides the temperature and process independent output voltage comprised of at least a differential output signal of the analog function means, the common mode voltage, and the bias voltage.

63. (Previously Presented) The integrated circuit of claim 58, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

64. (Previously Presented) The integrated circuit of claim 56, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

65. (Previously Presented) The integrated circuit of claim 56, wherein the analog function means comprises a circuit selected from the group consisting of multipliers, adaptive filters, modulators and neural networks.

66. (Previously Presented) The integrated circuit of claim 56, wherein the differential loading means comprises first and second loading means,

wherein the first loading means comprises a first terminal responsive to a first output terminal of the analog function means, a second terminal in communication with the common mode node, and a first control terminal,

wherein the second loading means comprises a third terminal responsive to a second output terminal of the analog function means, a fourth terminal in communication with the common mode node, and a second control terminal, and

wherein the biasing means is in communication with the first and second control terminals.

67. (Currently Amended) A method of performing an analog function, comprising the steps of:

a.) differentially loading the analog function;

b.) providing a common mode node to step (a.);

c.) providing a compensation signal to step (a.);

d.) providing a common mode voltage to step (a.) via the common mode node, wherein the common mode voltage is independent of temperature and manufacturing process variations; and

e.) providing the common mode voltage <u>and a plurality of control bias voltage signals</u> to step (c.).

68. (Previously Presented) The method of claim 67, wherein step (c.) further comprises the step of

f.) providing a bias voltage to step (a.),

wherein the bias voltage is independent of temperature and manufacturing process variations.

69. (Cancelled)

70. (Previously Presented) The method of claim 67, wherein the compensation signal provided by step (c.) varies the differential loading of step (a.).

71. (Previously Presented) The method of claim 67, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

72. (Previously Presented) The method of claim 67, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.